Q.P. Code: 16EC3807 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

I Year M.Tech II Semester R16 Regular Examinations May 2017

MICRO COMPUTER SYSTEM DESIGN

(DECS)

For Students admitted in 2016 only

Time: **3 hours** Max. Marks: **60**

Answer all Five Units **5 X 12 =60** Marks

UNIT-I

Q.1	a.	Explain the flag register of 8086.	5M
	b.	Explain about the segmentation concept in 8086.	7M
		OR	
Q.2	a.	Explain the internal architecture of 80286 with neat diagram.	7M
	b.	List the salient features of 80286..	5M
		UNIT-II	
Q.3	a.	Draw and discuss the paging mechanism of 80386	7M
	b.	Explain the procedure of converting a linear address in to a physical address.	5M
		OR	
Q.4	a.	Explain the special Pentium registers in detail.	7M
	b.	Write short notes on Super scalar architecture of Pentium.	5M
		UNIT-III	
Q.5	a.	Draw and discuss the micro architecture of Pentium IV	7M
	b.	What are the various registers available in Pentium 4 processor and explain.	5M
		OR	
Q.6	a.	Explain the implementation of Ready queue using FIFO scheduling policy.	7M
	b.	What is memory fragmentation? How it can be reduced.	5M
		UNIT-IV	
Q.7	a.	Draw and Explain the internal structure of 80x87 arithmetic co-processor.	7M
	b.	Explain the data transfer instructions of arithmetic co-processor.	5M
		OR	
Q.8	a.	Explain the 80x87 co-processor control register.	7M
	b.	Write short notes on floating point data format.	5M
		UNIT-V	
Q.9	a.	Explain the functional block diagram of 8096 with neat diagram.	7M
	b.	Explain the Port 2 functions of 8096.	5M
		OR	
Q.10	a.	Explain the addressing modes of 8096 with suitable examples	7M
	b.	Write short notes on PSW of 8096.	5M

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